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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,067	04/16/2004	Patrick Walsh	AD-352J	9968

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EXAMINER	
WANG, TED M	

ART UNIT	PAPER NUMBER
2611	

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01/24/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/826,067	WALSH ET AL.	
	Examiner	Art Unit	
	Ted M. Wang	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-12 and 14* is/are allowed.

6)☒ Claim(s) *13 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/12/2007 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claim13 have been considered but are moot in view of the new ground(s) of rejection.

3. Applicant's arguments, filed 12/12/2007, with respect to the rejection(s) of claim(s) 1-5, 7, 12 and 14 under 35 USC 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

4. Applicant's arguments, filed on 12/12/2007, with respect to claim 15, have been fully considered but they are not persuasive. The Examiner has thoroughly reviewed Applicants' arguments but firmly believes that the cited reference to reasonably and properly meet the claimed limitations.

Independent Claim 15

(1) *Applicants' argument* – "In support of the rejection of claim 15, the Examiner alleges that *Keaveney et al.* teaches that in fractional-N synthesizers, the output signal F out is only in phase with the input reference frequency every M periods of the

reference signal. To support this, the Examiner cites Col. 3, lines 34-59 *of Keaveney et al.* However, this section *of Keaveney et al.* relates to fractional-N synthesizers that are prior art to the invention of Keaveney et al. and not descriptive of the invention *of Keaveney et al.* itself, nor is it descriptive of Fig. 1 *of Keaveney et al. In* fact, the invention *of Keaveney et al.* overcomes the problems with the prior art by generating a synchronization pulse at integer multiples of periods of the reference signal. See *Keaveney et al.* at Col. 2, lines 1-33. Thus, in the rejection of claim 15, the Examiner is combining the invention *of Keaveney et al.* with the cited prior art *of Keaveney et al.*, when *Keaveney et al.* specifically teaches away from its cited prior art." as recited in lines 6-16 of Remarks, dated 12/12/2007.

Examiner's response – Column 3, lines 34-59 of Keaveney's references teaches that each time phase locked loop 12 is switched to a different channel, for example, interpolator being reset, that is, the frequency of its output, f_{OUT}, is changed by changing any one or more of the parameters F, M, N, the balancing process starts anew. In addition, Keaveney further teaches that in fractional-N synthesizers the higher frequency output signal f_{OUT} is only in phase with the input reference frequency 28 every M periods of the reference signal. That is, during the phase locked processing the phase of said output signal will be varied with respect to the phase of said input reference signal, f_{REF}.

(2) *Applicants' argument* – "Claim 15 as recited by the applicants includes the step of "generating a synchronization pulse at integer multiples of periods of the input reference

signal". The feature of generating synchronization pulses was taught by *Keaveney et al.*, but not its cited prior art. As noted above, the apparatus *of Keaveney et al.* includes the noted disadvantage that it can not be programmed to vary the phase of the output signal with respect to the phase of the input signal. As such, the subject invention of claim 15 includes the step of "generating an enable signal to reset an interpolator of said fractional-N synthesizer with said predetermined phase to vary the phase of said output signal with respect to the phase of said input reference signal". As such, claim 15 clearly distinguishes over *Keaveney et al.* and also over the prior art cited in *Keaveney et al.*" as recited in lines 6-16 of Remarks, dated 12/12/2007.

Examiner's response – Fig.1 element 40 and column 2 lines 26-33 of Keaveney's references clearly teaches generating a synchronization pulse (Fig.1 element 40) at integer multiples of periods of the input reference signal (Fig.1 element 28 and column 2 lines 26-33).

Thus, for the explanation addressed in the above paragraph, the rejection under 35 U.S.C. 102(e) with *Keaveney*'s reference is adequate.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claim 13 is rejected under 35 U.S.C. 102(a) as being anticipated by the admitted prior art of the instant application.

- With regard claim 13, the admitted prior art of the instant application teaches a method of varying the phase of the output signal with respect to the input reference signal of a fractional-N synthesizer (Fig.1 element 10), the method comprising the steps of:

  tracking an accumulated fractional phase (Fig.1 element F, M, interpolator 26, F/M, where the interpolator could be an accumulator (page 3 lines 8-9));

  scaling (Fig.1 element 24) the accumulated fractional phase by a predetermined phase value (Fig.1 element N); and

  loading the predetermined phase value into an interpolator and providing an output from the interpolator (Fig.1 element 50) to a frequency divider (Fig.1 element 22) to define a predetermined output frequency and phase (Fig.1 element 32) .

7. Claim 15 is rejected under 35 U.S.C. 102(e) as being anticipated by Keaveney et al. (US 6,556,086 B2).

- With regard claim 15, Keaveney et al., cited by the instant applicant, discloses a method of varying the phase of the output signal with respect to the input signal of a fractional-N synthesizer (Fig.1 element 10), the method comprising:

  generating a synchronization pulse (Fig.1 element 40) at integer multiples of periods of the input reference signal (Fig.1 element 28 and column 2 lines 26-33);

  generating a predetermined phase adjustment value (Fig.1 elements F, M, and F/M, column 1 lines 46-51, where F is the input fraction and M is the Modulus and both F and M are predetermined, column 1 lines 47-51); and

  generating an enable signal (Fig.1 elements 46 and 44 and column 4 lines 1-18) to reset (Fig.1 element 48 and column 4 lines 1-18) an interpolator (Fig.1 element 26) of said fractional-N synthesizer with said predetermined phase to vary the phase of said output signal with respect to said input reference signal (column 3 lines 35-59, where the frequency of its output, f_{OUT}, is changed by changing any one or more of the parameters F, M, N and received input frequency, since it is phase locked to the input frequency. Refer to Response to Arguments as addressed in the above paragraph.)

Allowable Subject Matter

8. Claims 1-12 and 14 are allowed.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted M. Wang whose telephone number is 571-272-3053. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ted M Wang
Examiner
Art Unit 2611

Ted M. Wang